EL979955718

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Methods Of Forming Trench Isolation Regions

* * * * *

INVENTORS:

Garo J. Derderian
H. Montgomery Manning

ATTORNEY'S DOCKET NO. MI22-2444

METHODS OF FORMING TRENCH ISOLATION REGIONS

TECHNICAL FIELD

[0001] This invention relates to methods of forming trench isolation regions.

BACKGROUND OF THE INVENTION

[0002] In typical semiconductor device applications, numerous devices are packed into a small area of a semiconductor substrate to create an integrated circuit. Many of the individual devices are electrically isolated from one another. Accordingly, electrical isolation is an integral part of semiconductor device design for preventing unwanted electrical coupling between adjacent components and devices.

[0003] Conventional methods of isolating circuit components typically use trench isolation regions. Such are formed by depositing or otherwise forming a masking layer over a semiconductor substrate. Trenches are etched through the masking layer into the semiconductor substrate, with the trenches being subsequently filled with insulative material. Exemplary

masking materials for trench isolation include silicon nitride and polysilicon with or without an underlying pad oxide layer. Further after forming the trenches, they are typically lined with silicon nitride which ultimately forms part of the trench isolation material. Sidewalls of the trenches are typically oxidized as well to form silicon dioxide and either before or after the nitride liner deposition.

[0004] The trench isolation material which is formed in the isolation trenches typically includes deposition of insulative material over the masking material and to within the trenches, typically over-filling them. The isolation material is typically then polished back, for example by chemical-mechanical polishing, at least to the outer surface of the masking material. The masking material is then typically selectively etched away from the substrate leaving, at least at this point in the process, insulative isolation material filling and extending outwardly of the trench isolation regions. Unfortunately where the masking material comprises silicon nitride and where silicon nitride is also utilized to line the trenches, the nitride liner might get etched as well. This can cause nitride liner recessing within the trenches relative to the outer surface of the semiconductive material of the substrate. This can result in gate oxide wrap-around that can degrade the transistors which are ultimately fabricated.

[0005] While the invention was motivated in addressing the above identified issues, it is in no way so limited. The invention is only limited by

the accompanying claims as literally worded, without interpretative or other limiting reference to the specification, and in accordance with the doctrine of equivalents.

SUMMARY

[0006] The invention includes methods of forming trench isolation regions. In one implementation, a masking material is formed over a semiconductor substrate. The masking material comprises at least one of tungsten, titanium nitride and amorphous carbon. An opening is formed through the masking material and into the semiconductor substrate effective to form an isolation trench within semiconductive material of the semiconductor substrate. A trench isolation material is formed within the isolation trench and over the masking material outside of the trench effective to overfill the isolation trench. The trench isolation material is polished at least to an outermost surface of the at least one of tungsten, titanium nitride and amorphous carbon of the masking material. The at least one of tungsten, titanium nitride and amorphous carbon is/are etched from the substrate.

[0007] In one implementation, a method of forming a trench isolation region comprises forming masking material over a semiconductor substrate, where at least some of the masking material is oxidizable. An opening is formed through the masking material and into the semiconductor substrate effective to form an isolation trench within semiconductive material of the semiconductor substrate. The opening and the isolation trench have respective sidewalls. The substrate is exposed to oxidizing conditions effective to oxidize the masking material sidewalls at a greater rate than

which the sidewalls of the semiconductive material are oxidized. Trench isolation material is formed within the isolation trench.

[0008] In one implementation, a method of forming a trench isolation region comprises forming a masking material over a semiconductor substrate. An opening is formed through the masking material and into the semiconductor substrate effective to form an isolation trench within semiconductive material of the semiconductor substrate. A silicon nitride comprising layer is deposited within the isolation trench and over the masking material effective to line the trench. Trench isolation material is deposited over the silicon nitride comprising layer within the isolation trench and over the masking material outside of the trench. The trench isolation material and the silicon nitride comprising layer are polished at least to the masking material. The masking material and the trench isolation material are removed relative to the silicon nitride comprising layer from outwardly of semiconductive material of the semiconductor substrate effective to leave a portion of the silicon nitride comprising layer projecting outwardly from semiconductive material of the semiconductor substrate.

[0009] Other implementations and aspects are contemplated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0011] Fig. 1 is a diagrammatic section view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

[0012] Fig. 2 is a view of the Fig. 1 wafer fragment at a processing subsequent to that depicted by Fig. 1.

[0013] Fig. 3 is a view of the Fig. 2 wafer fragment at a processing subsequent to that depicted by Fig. 2.

[0014] Fig. 4 is a view of the Fig. 3 wafer fragment at a processing subsequent to that depicted by Fig. 3.

[0015] Fig. 5 is a view of the Fig. 4 wafer fragment at a processing subsequent to that depicted by Fig. 4.

[0016] Fig. 6 is a diagrammatic section view of another semiconductor wafer fragment in process in accordance with an aspect of the invention.

[0017] Fig. 7 is a diagrammatic section view of another semiconductor wafer fragment in process in accordance with an aspect of the invention.

[0018] Fig. 8 is a view of the Fig. 7 wafer fragment at a processing subsequent to that depicted by Fig. 7.

[0019] Fig. 9 is a view of the Fig. 8 wafer fragment at a processing subsequent to that depicted by Fig. 8.

[0020] Fig. 10 is a diagrammatic section view of another semiconductor wafer fragment in process in accordance with an aspect of the invention.

[0021] Fig. 11 is a view of the Fig. 10 wafer fragment at a processing subsequent to that depicted by Fig. 10.

[0022] Fig. 12 is a view of the Fig. 11 wafer fragment at a processing subsequent to that depicted by Fig. 11.

[0023] Fig. 13 is a view of the Fig. 12 wafer fragment at a processing subsequent to that depicted by Fig. 12.

[0024] Fig. 14 is a diagrammatic section view of another semiconductor wafer fragment in process in accordance with an aspect of the invention.

[0025] Fig. 15 is a view of the Fig. 14 wafer fragment at a processing subsequent to that depicted by Fig. 14.

[0026] Fig. 16 is a diagrammatic section view of another semiconductor wafer fragment in process in accordance with an aspect of the invention.

[0027] Fig. 17 is a view of the Fig. 16 wafer fragment at a processing subsequent to that depicted by Fig. 16.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[0029] An exemplary embodiment method of forming a trench isolation region is initially described with reference to Figs. 1-5. Fig. 1 depicts a semiconductor substrate 10 comprising bulk semiconductive material 12, for example monocrystalline silicon. Although the invention is described throughout in the preferred context of bulk semiconductor processing, semiconductor-on-insulator fabrication methods as well as any other methods of fabricating trench isolation regions are contemplated in accordance with the invention. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Further in the context of this document, the term "layer" encompasses both the singular and the plural.

[0030] A masking material 14 is formed over and comprises semiconductor substrate 10. In the depicted exemplary embodiment, such comprises a pad oxide layer 16 and a layer 18 formed thereover. An exemplary thickness for layer 16 is from 20 Angstroms to 75 Angstroms, with 60 Angstroms being a preferred specific example. Masking material layer 18 preferably has a thickness of from 200 Angstroms to 1,500 Angstroms, with 500 Angstroms being a specific preferred example. Masking material layer 18 comprises at least one of tungsten (in elemental and/or alloy form), titanium nitride and amorphous carbon. In one embodiment where amorphous carbon is utilized, it might comprise at least one of boron and nitrogen.

[0031] Further in one exemplary embodiment with respect to amorphous carbon, such might comprise a layer that is transparent to visible light. In the context of this document, an amorphous carbon comprising layer that is transparent to visible light means that the amorphous carbon comprising layer has a substantially low absorption coefficient (k) in which k has a range between about 0.15 and about 0.001 (or lower) at wavelength 633 nm. The amorphous carbon comprising layer transparent to visible light range radiation, by way of example only, might be formed at a temperature from about 200°C to about 450°C, with an exemplary preferred pressure range being from about 3 Torr to about 7 Torr. A specific preferred example is 375°C and 5 Torr. Such deposition preferably occurs by plasma generation, with an exemplary power applied to the showerhead being

from 500 watts to 1100 watts, with 800 watts being a specific preferred example. An exemplary flow rate for the C_3H_6 is from 400 sccm to 2400 sccm, with 1450 sccm being a specific preferred example. An exemplary preferred flow rate for the helium is from 250 sccm to 650 sccm, with 450 sccm being a specific preferred example. An exemplary preferred spacing of the showerhead/substrate support-susceptor is 240 mils. Exemplary additional or other hydrocarbon gases utilizable in producing transparency as described include CH_4, C_2H_2, C_2H_4, C_2H_6, and C_3H_8. A preferred gas provided during such deposition might be either one gas or a combination of various gases, including the absence of any helium. Further, lower temperature depositions can result in greater transparency than higher temperature depositions. By way of example only, an exemplary deposition thickness over the substrate for the amorphous carbon comprising layer is 4000 Angstroms. If boron and/or nitrogen doping of the amorphous carbon comprising layer is desired, an exemplary boron source gas is B_2H_6 at an exemplary flow rate of 1500 sccm, and an exemplary nitrogen source gas is N_2 at an exemplary flow rate of 1000 sccm. Where boron doping is desired, an exemplary concentration range in the layer for boron is from 0.5% atomic to 60% atomic. Where nitrogen doping is desired, an exemplary concentration range in the layer for nitrogen is from 0.1% atomic to 20% atomic.

[0032] Hard masking and/or antireflective coating layers might be utilized over masking material layer 18. In one preferred embodiment, masking material 14 is void of silicon nitride.

[0033] Referring to Fig. 2, an opening 20 has been formed through masking material 14 into semiconductor substrate 10 effective to form an isolation trench 22 within semiconductive material 12 of semiconductor substrate 10. An exemplary preferred manner of doing so is by photolithographic patterning, development and etching, whether using existing or yet-to-be developed technologies.

[0034] Referring to Fig. 3, trench isolation material 24 has been formed within isolation trench 22 and over masking material 14 outside of trench 22 effective to overfill isolation trench 22. An exemplary preferred material is silicon dioxide, for example high density plasma deposited silicon dioxide, and further, for example, with or without thermal oxide and/or silicon nitride trench liner materials.

[0035] Referring to Fig. 4, trench isolation material 24 has been polished at least to an outermost surface of the at least one of tungsten, tungsten nitride and amorphous carbon material 18 of masking material 14. Exemplary preferred techniques include chemical-mechanical polishing, for example utilizing any existing or yet-to-be developed CMP tool and slurries.

[0036] Referring to Fig. 5, the at least one of tungsten, titanium nitride and amorphous carbon material 18 has been etched from the substrate. Preferably, the etching is conducted selectively to at least some of trench isolation material 24, with the etching as shown being selective to all of trench isolation material 24. In the context of this document, a selective etch or removal removes one material compared to another at a ratio of at least 2:1. The exemplary pad oxide layer 16 might also be removed, as well as some or all of material 24 from outwardly of isolation trench 22.

[0037] By way of example only, an alternate exemplary embodiment to that depicted by Fig. 4 is illustrated in Fig. 6 in connection with a semiconductor substrate 10a. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with different numerals or with the suffix "a". Masking material 14a comprises at least two of tungsten, titanium nitride and amorphous carbon with, for example, an outer layer 19 of at least one of such materials being received outwardly of masking material layer 18a which comprises another of at least one of tungsten, titanium nitride and amorphous carbon. In one exemplary embodiment, material 19 preferably comprises amorphous carbon and material 18a comprises at least one of tungsten and tungsten nitride.

[0038] By way of example only, another exemplary embodiment method of forming a trench isolation region is described with reference to Figs. 7-9 in connection with a semiconductor substrate 10b. Like numerals from the

first-described embodiment are utilized where appropriate, with differences being indicated with different numerals or with the suffix "b". Referring to Fig. 7, trench isolation material 24b has been formed within isolation trench 22 and over masking material 14 outside of trench 22 effective to overfill isolation trench 22. Trench isolation material 24b includes a silicon nitride comprising layer 30 and at least one material 32 other than silicon nitride formed thereover. An exemplary thickness for layer 30 is 70 Angstroms, and an exemplary preferred material for layer 32 is high density plasma deposited silicon dioxide. Of course, a thermal silicon dioxide layer might be formed on trench sidewalls 22 before or after deposition of layer 30.

[0039] Referring to Fig. 8, trench isolation material 24b has been polished to at least an outermost surface of the at least one of tungsten, titanium nitride and amorphous carbon material 18 of masking material 14.

[0040] Referring to Fig. 9, the at least one of tungsten, titanium nitride and amorphous carbon material 18 has been etched from the substrate substantially selectively to silicon nitride comprising layer 30. By way of example only, an exemplary etching chemistry for etching elemental tungsten, amorphous carbon, and/or TiN selectively relative to silicon nitride comprises H_2SO_4 and H_2O_2 at a 9:1 ratio by weight at 140°C. Further by way of example only, an exemplary etching chemistry for etching elemental

tungsten and/or TiN selectively relative to silicon nitride comprises H_2O, HCl, and H_2O_2 at a 20:4:1 ratio by weight at 70°C.

[0041] Yet another exemplary method of forming a trench isolation region is described in connection with Figs. 10-13 in connection with a semiconductor substrate 10c. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with different numerals or with the suffix "c". Referring initially to Fig. 10, a masking material 14c has been formed over semiconductor substrate 12. Such is depicted as comprising a pad oxide layer 16 and an overlying material 18c, at least some of which is oxidizable. Thicknesses are preferably as described above in connection with the first described embodiment. Exemplary materials include those as described above, specifically tungsten, amorphous carbon, and/or tungsten nitride. An additional alternate exemplary material is polysilicon, whether updoped or doped with another material or materials such as boron and/or phosphorus. Additional oxidizable masking materials are contemplated, whether existing or yet-to-be developed. Regardless, in one exemplary preferred embodiment, masking material 14c is void of silicon nitride.

[0042] Referring to Fig. 10, an opening 20 is formed through masking material 14c and into semiconductor substrate 10c effective to form an isolation trench 22 within semiconductive material 12 of semiconductor

substrate 10c. Mask opening 20 has sidewalls 34, and isolation trench 22 has sidewalls 36.

[0043] Referring to Fig. 11, substrate 10c has been exposed to oxidizing conditions effective to oxidize masking material sidewalls 34 at a greater rate than that at which sidewalls 36 of semiconductor material 12 are oxidized. Thereby in one preferred embodiment, an oxide layer 39 is formed which is laterally thicker over the masking material sidewalls within opening 20 than over the sidewalls of semiconductive material 12.

[0044] Referring to Fig. 12, trench isolation material 24c has been formed within isolation trench 22. Such might comprise one or more materials, with material 39 also comprising trench isolation material. Processing might otherwise continue as described above in connection with the first-described embodiments, for example whereby materials 24c, 39 and 14c are removed outwardly from semiconductive material 12, for example as shown in Fig. 13.

[0045] An alternate exemplary embodiment semiconductor substrate 10d is depicted in Figs. 14 and 15. Like numerals from the Figs. 10-13 embodiment are utilized where appropriate, with differences being indicated with different numerals or with the suffix "d". Referring to Fig. 14, Semiconductor substrate 10d is shown as being formed to comprise trench isolation material 24d comprising a silicon nitride

comprising layer 42 received over (and "on", as shown) the oxidized masking material sidewalls and oxidized semiconductive material sidewalls (i.e., on material 39). An exemplary additional material 44 is formed thereover, for example high density plasma deposited silicon dioxide.

[0046] Referring to Fig. 15, and by way of example only, subsequent processing is depicted whereby all material has been removed outwardly from material 12 of semiconductor substrate 10d.

[0047] Yet another preferred method of forming a trench isolation region in accordance with aspects of the invention is described in connection with a semiconductor substrate 10e in Figs. 16 and 17. Like numerals from the first-described embodiments are utilized where appropriate, with differences being indicated with different numerals or with the suffix "e". Referring to Fig. 16, a masking material 14 is formed over a semiconductor substrate 12. Any material is contemplated, and including for example those described above, and preferably with such masking material being void of silicon nitride. An opening 20 has been formed through masking material 14 and into semiconductor material 12 effective to form an isolation trench 22 within material 12 of semiconductor substrate 10e. A silicon nitride comprising layer 50 has been deposited within isolation trench 22 and over masking material 14 effective to line trench 22. An exemplary thickness for layer 50 is from 10 Angstroms to 150 Angstroms. Trench isolation material 24 has been deposited over silicon nitride

comprising layer 50 within isolation trench 22 and over masking material 14 outside of trench 22. Exemplary preferred materials are as described above, namely high density plasma deposited silicon dioxide. Fig. 16 depicts such trench isolation material 24 and silicon nitride comprising layer 50 as having been polished at least to masking material 14.

[0048] Referring to Fig. 17, masking material 14 and trench isolation material 24 have been removed relative to silicon nitride comprising layer 50 from outwardly of semiconductive material 12 of semiconductive substrate 10e effective to leave a portion of silicon nitride comprising layer 50 projecting outwardly of semiconductive material 12 of semiconductive substrate 10e. An exemplary technique for such processing, where for example material 24 is silicon dioxide and material 18 is polysilicon includes dipping or spraying with a 25:1 by volume solution of H_2O:HF at room temperature and pressure conditions. Alternately with polysilicon and silicon dioxide, such a solution could be utilized initially to strip any native oxide overlying material 18 followed by etching polysilicon with tetramethyl ammonium hydroxide (TMAH). An exemplary such solution is 2.25% TMAH by weight in deionized water at 30°C.

[0049] In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed

comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.